PRELIMINARY

CCG1 Datasheet

USB Type-C Port Controller with Power Delivery

General Description

CCG1 provides a complete USB Type-C and USB Power Delivery port control solution. The scalable and reconfigurable core architecture of CCG1 enables a base Type-C solution that can scale to a complete 100-W USB Power Delivery with Alternate Mode mux support. CCG1 is also a Type-C cable ID IC for active and passive cables. The ARM® Cortex®-M0 CPU based core can use common open source firmware or custom solutions developed with common libraries and APIs. CCG1 is the CC controller that detects connector insert, plug orientation, and V_{CONN} switching signals. CCG1 makes it easier to add USB Power Delivery to any architecture because it provides the control signals to manage external VBUS and V_{CONN} power management solutions as well as external mux controls for most single cable-docking solutions. CCG1's packaging options, and programmability, enables any USB Type-C and USB Power Delivery solution.

Applications

- Notebooks, tablets, monitors, docking stations
- Power adapters, USB Type-C cables

Features

32-bit MCU Subsystem

- 48-MHz ARM Cortex-M0 CPU with 32-KB flash and 4-KB SRAM

Integrated analog blocks

- 12-bit, 1-Msps ADC for VBUS voltage and current monitoring
- Dynamic overcurrent and overvoltage protection

Integrated digital blocks

- Two configurable 16-bit TCPWM blocks
- One I^2C master or slave

Type-C Support

- Integrated transceiver (BB PHY)
- Supports up to two USB ports with PD
- Supports routing of all protocols through an external mux

PD Support

- Supports Provider and Consumer roles
- Supports all power profiles

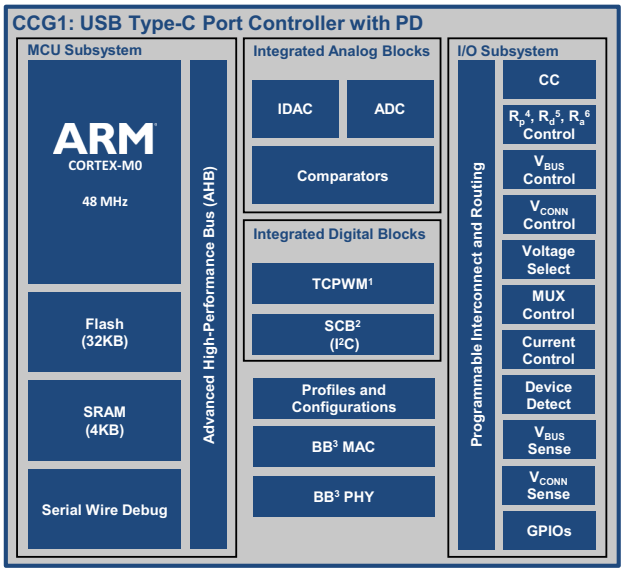
Low power operation

- 1.8-V to 5.5-V operation
- Sleep 1.3 mA, Deep Sleep 1.3 uA

Packages

- 40-pin QFN
- 16-pin SOIC
- 35-ball wafer-level CSP (WLCSP)

Figure 1. CCG1 Block Diagram [1, 2, 3, 4, 5, 6]



Notes

1. Timer, counter, pulse-width modulation block.
2. Serial communication block configurable as I^2C.
3. Base band.
4. Termination resistor denoting a Downstream Facing Port (DFP).
5. Termination resistor denoting a Upstream Facing Port (UFP).
6. Termination resistor denoting an Electronically Marked Cable Assembly (EMCA).

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Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in the CCG1 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for CCG1 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The CCG1 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section Power on page 12. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) or interrupts (Low Voltage Detect (LVD)). The CCG1 operates with a single external supply over the range of 1.8 to 5.5 V and has three different power modes: Active, Sleep, and Deep Sleep; transitions between modes are managed by the power system.

Serial Communication Blocks (SCB)

The CCG1 has one SCB, which can implement an I^2C interface. The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZ-I^2C that creates a mailbox address range in the memory of the CCG1 and effectively reduces I^2C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripheral is compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices, as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

The CCG1 is not completely compliant with the I^2C spec in the following respects:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8 mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the Bus Load.
- When the SCB is an I^2C Master, it interposes an IDLE state between NACK and Repeated Start; the I^2C spec defines Bus free as following a Stop condition so other Active Masters do not intervene but a Master that has just become activated may start an Arbitration cycle.
- When the SCB is in the I^2C Slave mode, and Address Match on External Clock is enabled (EC_AM = 1) along with operation in the internally clocked mode (EC_OP = 0), then its I^2C address must be even.

GPIO

The CCG1 has 34 GPIOs, which are configured for various functions. Refer to the pinout tables for the definitions. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode).
- Selectable slew rates for dV/dt related noise control to improve EMI.

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network, known as a high-speed I/O matrix, is used to multiplex between various signals that may connect to an I/O pin.

Pin Definitions

Following is the pin definition #1 for 35-Ball WLCSP for the Cable/EMCA application. Refer to Table 22 for part numbers to package mapping.

Table 1. Pin Definitions for 35-ball WLCSP for EMCA Cable Application

Functional Pin Name	35-WLCSP#1 Balls	Type	Description
CC1_RX	C4	I	CC1 control 0: TX enabled z: RX sense
CC1_TX	D7	O	Configuration Channel 1
SWD_IO	D1	I/O	SWD I/O
SWD_CLK	C1	I	SWD clock
I2C_SCL	B1	I/O	I^2C clock signal
I2C_SDA	B2	I/O	I^2C data signal
XRES	B6	I	Reset
VCCD	A7	POWER	Regulated digital supply output. Connect a 1 to 1.6-µF capacitor. No external source should be connected
VDDD	C7	POWER	Power supply for both analog and digital sections
VSSA	B7	GND	Analog ground
CC_VREF	C5	I	Data reference signal for CC lines
TX_U	B3	O	Signals for internal use only. The TX_U output signal should be connected to the TX_M signal
TX_M	B5	I	
TX_REF_IN	D3	I	Reference signal for internal use. Connect to TX_REF output via a 2.4K 1% resistor
TX_GND	A3	I	Connect to GND via 2K 1% resistor
TX_REF_OUT	D4	O	Reference signal generated by connecting internal current source to two 1K external resistors
RA_DISCONNECT	E4	O	Optional control signal to remove RA after assertion of VCONN 0: RA disconnected 1: RA connected
VCONN_DET	C6	I	Local VCONN detection signal 0: VCONN is not locally applied 1: VCONN is locally applied
CC1_LPREF	A5	I	Reference signal for internal use. Connect to the output of resistor divider from VDDD.
RA_FAR_DISCONNECT	E5	O	Optional control signal to remove RA after assertion of VCONN (NC for 2 chip/cable) 0: RA disconnected 1: RA connected
BYPASS	D5	I	Bypass capacitor for internal analog circuits
CC1_LPRX	C3	I	Configuration channel 1 RX signal for Low Power States
GPIO	A1, A2, A4, A6, B4, C2, D2, D6, E1, E2, E3, E6, E7	–	General-purpose I/Os

Following is the pin definitions for 40-pin QFN and 35-ball WLCSP for the notebook, tablet, smartphone, and monitor applications. Refer to Table 22 for part numbers to package mapping.

Functional Pins	40-QFN#1 Pins	40-QFN#2 Pins	35-CSP#2 Balls	Type	Description
MUXSEL_1	1	1	D5	O	External Data Mux Select signal 1
MUXSEL_2	2	2	D6	O	External Data Mux Select signal 2
CC1_CTRL	3	3	D3	I/O	CC1 control 0: TX enabled z: RX sense
CC2_CTRL	4	4	E4	I/O	CC2 control 0: TX enabled z: RX sense
MUXSEL_3	5	5	E5	O	External Data Mux Select signal 3
MUXSEL_4	6	6	E6	O	External Data Mux Select signal 4
CS_P	7	7	E3	I	Current Sensing Plus input
CS_M	8	8	E2	I	Current Sensing Minus input I
VSS	9	9	–	GND	Ground
CC1	10	10	E1	I/O	Configuration Channel 1
MUXSEL_5	11	11	D2	O	External Data Mux Select signal 5
SWD_IO	12	12	D1	I/O	SWD IO
SWD_CLK	13	13	C1	I	SWD Clock
HOTPLUG_DET	14	14	C2	I/O	HotPlug Detection for Display Port Alternate Mode
GPIO1	15	–	–	I/O	GPIO
VSEL2	–	15	–	O	Voltage Select signal 2 for selecting output voltage
GPIO2	16	–	–	I/O	GPIO IO
C_SEL	–	16	–	I	Configuration Select signal
GPIO3	17	–	–	I/O	GPIO
IFAULT	–	17	–	I	Current Fault Indication 0: No fault 1: Current fault
I2C_SCL	18	18	B1	I/O	I2C Clock signal
I2C_SDA	19	19	B2	I/O	I2C Data signal
I2C_INT	20	20	A2	O	I2C Interrupt
DEV_DET	21	21	A1	O	Device detection signal indicating the attached device type
CC1_RD	22	22	C3	O	Open Drain signal to connect RD to CC 1 line z: RD not connected 0: RD connected
CC1_RP	23	23	A5	O	Open Source signal to connect RP to CC 1 line z: RP not connected 1: RP connected

Functional Pins	40-QFN#1 Pins	40-QFN#2 Pins	35-CSP#2 Balls	Type	Description
CC1_VCONN_CTRL	24	24	A4	O	Open Drain signal to control a PFET power switch for VCONN on CC 1 line 0: VCONN switch closed z: VCONN switch open
VBUS_DISCHARGE	25	25	A3	O	Signal used for discharging VBUS line during voltage change
CC2	26	26	B3	O	Configuration Channel 2
CC2_RD	27	27	A6	O	Open Drain signal to connect RD to CC 2 line z: RD not connected 0: RD connected
CC2_RP	28	28	B4	O	Open Source signal to connect RP to CC 2 line z: RP not connected 1: RP connected
CC2_VCONN_CTRL	29	29	B5	O	Open Drain signal to control a PFET power switch for VCONN on CC 2 line 0: VCONN switch closed z: VCONN switch open
XRES	30	30	B6	I	Reset
VCCD	31	31	A7	POWER	Regulated digital supply output. Connect a 1 to 1.6-µF capacitor. No external source should be connected
VDDD	32	32	C7	POWER	Power supply for digital sections
VDDA	33	33	C7	POWER	Power Supply for analog sections
VSSA	34	34	B7	GND	Analog ground pin
VBUS_VMON	35	35	C4	I	VBUS Overvoltage Protection monitoring signal
VBUS_VREF	36	36	C5	I	VBUS reference signal for Overvoltage Protection detection
VSEL1	37	37	C6	O	Voltage Select signal 1 for selecting the output voltage
VBUS_C_CTRL	38	–	D7	O	Full rail control signal for enabling/disabling Consumer load FET
VBUS_OK	–	38	–		VBUS_OK=1 - VBUS Voltage ok VBUS_OK=0 - VBUS Overvoltage detected
CC_VREF	39	39	D4	I	Data reference signal for CC lines
VBUS_P_CTRL	40	40	E7	O	Full rail control signal for enabling/disabling Provider load FET

Following is the pin definition for 40-pin QFN for Notebook (DFP) application. Refer to Table 22 for part numbers to package mapping.

Table 2. Pin Definitions for 40-Pin QFN for Notebook (DFP)

Functional Pin Name	Active HIGH/ LOW	Drive Mode	PSoC4A Port for 40-QFN	40-QFN #3 Pins	Type	Description
MUXSEL_1	-	Open drain, drives low	P2.0	1	O	External Data Mux Select signal 1
MUXSEL_2	-	Open drain, drives low	P2.1	2	O	External Data Mux Select signal 2
CC1_CTRL	-	Analog input/Strong drive (push pull)	P2.2	3	IO	CC1 control 0:Tx enabled z: RX sense
CC2_CTRL	-	Analog input/Strong drive (push pull)	P2.3	4	IO	CC2 control 0: TX enabled z: RX sense
MUXSEL_3	-	Open drain, drives low	P2.4	5	O	External Data Mux Select signal 3
MUXSEL_4	-	Open drain, drives low	P2.5	6	O	External Data Mux Select signal 4
CS_P	-	Analog input	P2.6	7	I	Current Sensing Plus input
CS_M	-	Analog input	P2.7	8	I	Current Sensing Minus input
VSS	-	-	VSS	9	GND	Ground
CC1	-	Strong drive (push pull)	P3.0	10	O	Configuration Channel 1
CC1_RP_1.5	Active HIGH	Open drain, drives high	P3.1	11	O	Open Drain signal to connect RP to CC1 line (1.5A current) z: RP not connected 1: RP connected
SWD_IO	-	-	P3.2	12	IO	SWD IO
SWD_CLK	-	-	P3.3	13	I	SWD Clock
CC1_RP_3.0	Active HIGH	Open drain, drives high	P3.4	14	O	Open Source signal to connect RP to CC1 line (3A current) z: RP not connected 1: RP connected
CC1_RP_DEF	Active HIGH	Open drain, drives high	P3.5	15	O	Open Drain signal to connect RP to CC1 line (Default current) z: RP not connected 1: RP connected
CC2_RP_DEF	Active HIGH	Open drain, drives high	P3.6	16	O	Open Drain signal to connect RP to CC2 line (Default current) z: RP not connected 1: RP connected
CC2_RP_1.5	Active HIGH	Open drain, drives high	P3.7	17	O	Open Drain signal to connect RP to CC2 line (1.5A current) z: RP not connected 1: RP connected
I2C_SCL	Active LOW	Open drain, drives low	P4.0	18	IO	I^2C Clock signal
I2C_SDA	Active LOW	Open drain, drives low	P4.1	19	IO	I^2C Data signal
I2C_INT	Active LOW	Open drain, drives low	P4.2	20	O	I^2C Interrupt

Table 2. Pin Definitions for 40-Pin QFN for Notebook (DFP) *(continued)*

Functional Pin Name	Active HIGH/ LOW	Drive Mode	PSoC4A Port for 40-QFN	40-QFN #3 Pins	Type	Description
CC2_RP_3.0	Active HIGH	Open drain, drives high	P4.3	21	O	Open Source signal to connect RP to CC2 line (3A current) z: RP not connected 1: RP connected
CC1_LPRX	-	Analog input	P0.0	22	I	Configuration channel 1 RX signal for Low Power States
CC1_LPREF	-	Analog input	P0.1	23	I	Reference signal for internal use.
CC2_LPRX	-	Analog input	P0.2	24	I	Configuration channel 2 RX signal for Low Power States
CC2_LPREF	-	Analog input	P0.3	25	I	Reference signal for internal use.
CC2	-	Strong drive (push pull)	P0.4	26	O	Configuration Channel 2
CC1_VCONN_ CTRL	Active LOW	Open drain, drives low	P0.5	27	O	Open Drain signal to control a PFET power switch for VCONN on CC1 line 0: VCONN switch closed z: VCONN switch open
CC2_VCONN_ CTRL	Active LOW	Open drain, drives low	P0.6	28	O	Open Drain signal to control a PFET power switch for VCONN on CC2 line 0: VCONN switch closed z: VCONN switch open
IFAULT	Active HIGH	Digital input	P0.7	29	I	Current Fault Indication on VBUS 0: No fault 1: Over Current fault
XRES	Active LOW	Analog input	XRES	30	I	Reset
VCCD	-	-	VCCD	31	POWE R	Connect 1uf Capacitor between VCCD and Ground
VDDD	-	-	VDDD	32	POWE R	5-V Supply
VDDA	-	-	VDDA	33	POWE R	5-V Supply
VSSA	-	-	VSSA	34	GND	
E-PAD	-	-	E-PAD	E-PAD	GND	
VBUS_VMON	-	Analog input	P1.0	35	I	VBUS Over-voltage Protection monitoring signal
VBUS_VREF	-	Analog input	P1.1	36	I	VBUS reference signal for Over-voltage Protection detection
VBUS_P_CTRL	Active HIGH	Strong drive (Push Pull)	P1.2	37	O	Full rail control signal for enabling/disabling Provider load FET
HOTPLUG_DE T	Active HIGH	Open drain, drives low	P1.3	38	IO	HotPlug Detection for Display Port Alternate Mode
CC_VREF/VBU S_DISCHARGE	-/Active High	Analog input/Strong drive (Push Pull)	P1.4	39	IO	Data reference signal for CC lines / Signal used for discharging VBUS line during voltage change

Table 2. Pin Definitions for 40-Pin QFN for Notebook (DFP) *(continued)*

Functional Pin Name	Active HIGH/ LOW	Drive Mode	PSoC4A Port for 40-QFN	40-QFN #3 Pins	Type	Description
MUXSEL_5	-	Open drain, drives low	P1.7	40	O	External Data Mux Select signal 5

Following is the pin definition for 16-pin SOIC for the Power Adapter application. Refer to Table 22 for part numbers to package mapping

Table 3. Pin Definitions for 16-pin SOIC for Power Adapter Application

Functional Pin Name	16-pin SOIC Pins	Type	Description
SWD_CLK	1	I	SWD Clock
VBUS_P_CTRL	2	O	Full rail control signal for enabling/disabling provider load FET
VBUS_VMON	3	I	VBUS over-voltage protection monitoring signal
VBUS_VREF	4	I	VBUS reference signal for over-voltage protection detection
XRES	5	–	Active Low Reset
VCCD	6	–	Connect 1 µF capacitor between VCCD and GROUND
VSSD	7	–	Ground
VDDD	8	–	Power 3.3 V/5 V
VSSA	9	–	Ground
CC_VREF/VBUS_DISCHARGE	10	I/O	Data reference signal for CC line (0.55 Volt) / Signal used for discharging VBUS line during voltage decrease
CC_CTRL	11	I/O	CC1 control 0: TX enabled z: RX sense
CS	12	I	Low Side Current Sense
VSEL1	13	O	Voltage select signal for selecting the output voltage 5/12/20 V
VSEL2	14	O	Voltage select signal for selecting the output voltage 5/12/20 V
CC	15	I/O	Configuration Channel TX/RX
SWD_IO	16	I/O	SWD I/O

Pinouts

Figure 2. 40-pin QFN Pinout

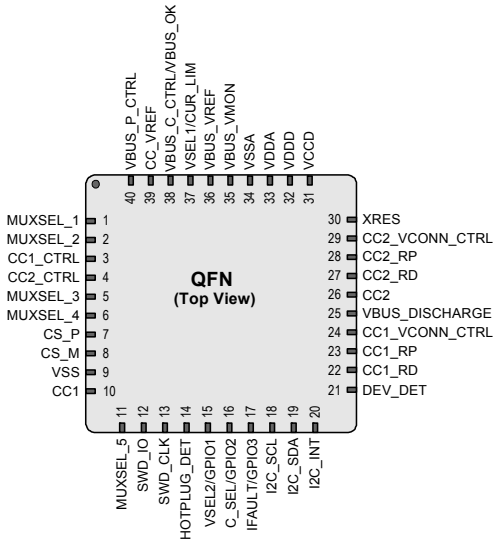


Figure 3. 16-pin SOIC Pinout

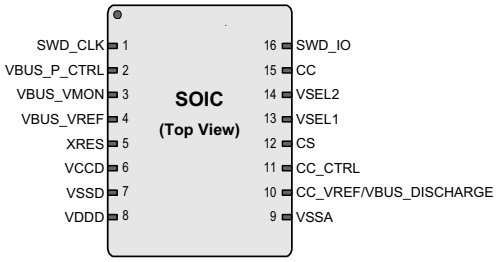
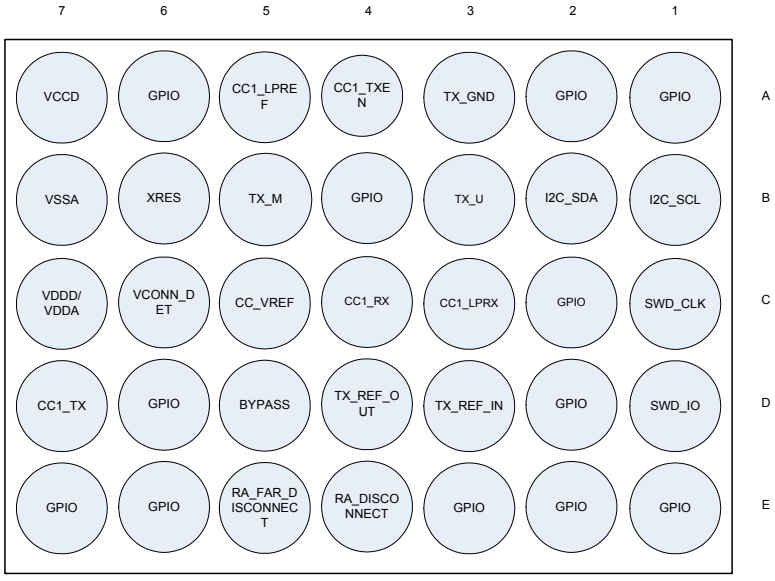


Figure 4. 35-Ball WLCSP Pinout


7 6 5 4 3 2 1
A: VCCD | GPIO | CC1_LPREF | CC1_TXEN | TX_GND | GPIO | GPIO
B: VSSA | XRES | TX_M | GPIO | TX_U | I2C_SDA | I2C_SCL
C: VDDD/VDDA | VCONN_DET | CC_VREF | CC1_RX | CC1_LPRX | GPIO | SWD_CLK
D: CC1_TX | GPIO | BYPASS | TX_REF_OUT | TX_REF_IN | GPIO | SWD_IO
E: GPIO | GPIO | RA_FAR_DISCONNECT | RA_DISCONNECT | GPIO | GPIO | GPIO

Power

The following power system diagram shows the minimum set of power supply pins as implemented for the CCG1. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the VDDA input. There is a separate regulator for the Deep Sleep mode. There is a separate low-noise regulator for the bandgap. The supply voltage range is 1.8 to 5.5 V with all functions and circuits operating over that range.

The CCG1 is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the CCG1 supplies the internal logic and the VCCD output of the CCG1 must be bypassed to ground via an external capacitor (in the range of 1 to 1.6 µF; X5R ceramic or better). No voltage source should be applied to this pin.

VDDA and VDDD must be shorted together; the grounds, VSSA and VSS must also be shorted together. Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Examples of bypass schemes follow.

Figure 5. 40-pin QFN Example

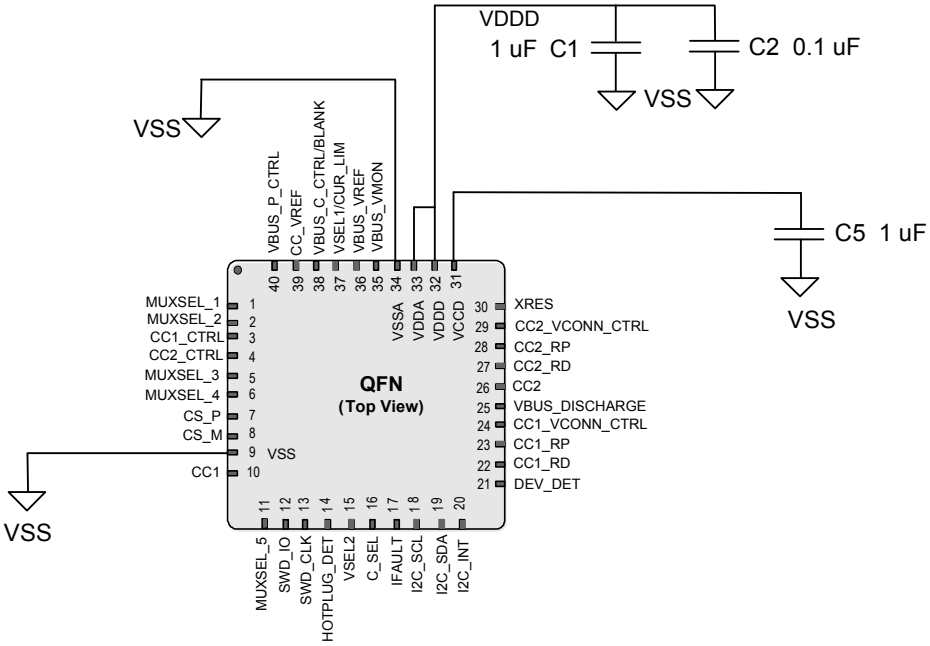


Figure 6. 16-pin SOIC Example

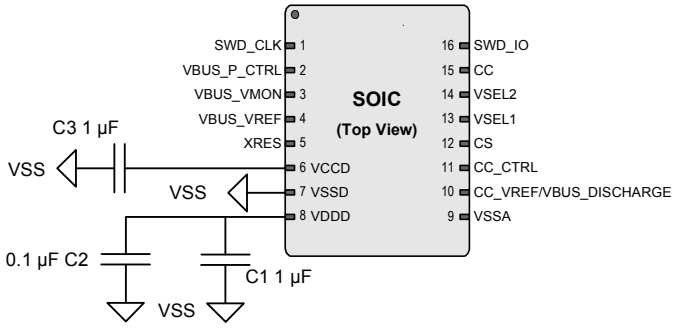
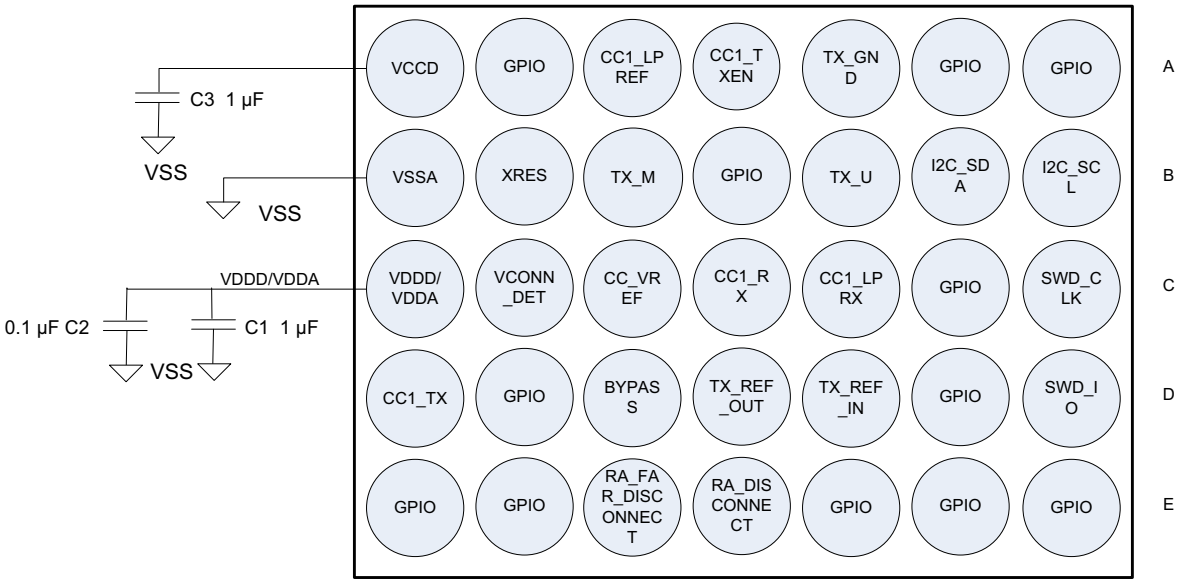


Figure 7. 35-ball WLCSP Example



Electrical Specifications

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings[7]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V_{DDD_ABS}	Digital supply relative to V_{SSD}	–0.5	–	6.0	V	Absolute max
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	–0.5	–	1.95	V	Absolute max
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DDD}+0.5	V	Absolute max
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25.0	–	25.0	mA	Absolute max
SID5	$I_{GPIO\_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.50	–	0.5	mA	Absolute max, current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	
BID46	LU	Pin current for latch-up	–200	–	200	mA	

Device Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C for 35-CSP and 40-QFN package options. Specifications are valid for –40 °C ≤ T_A≤ 105 °C and T_J≤120 °C for 16-SOIC package options. Specifications are valid for 1.8 V to 5.5 V, except where noted.

Table 5. DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	V_{DDD}	Power supply input voltage	1.8	–	5.5	V	With regulator enabled
SID54	V_{CCD}	Output voltage (for core logic)	–	1.8	–	V	
SID55	C_{EFC}	External regulator voltage bypass	1.0	1.3	1.6	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply decoupling capacitor	–	1.0	–	µF	X5R ceramic or better
Active Mode, V_{DDD} = 1.8 to 5.5 V. Typical values measured at V_{DD} = 3.3 V.							
SID19	I_{DD14}	Execute from flash; CPU at 48 MHz	–	12.8	–	mA	T = 25 °C
SID20	I_{DD15}	Execute from flash; CPU at 48 MHz	–	–	13.8	mA	
Sleep Mode, V_{DDD} = 1.8 to 5.5 V							
SID25A	I_{DD20A}	I^2C wakeup and comparators on	–	1.7	2.2	mA	
Deep Sleep Mode, V_{DDD} = 1.8 to 3.6 V (Regulator on)							
SID31	I_{DD26}	I^2C wakeup on	–	1.3	–	µA	T = 25 °C, 3.6 V
SID32	I_{DD27}	I^2C wakeup on	–	–	50.0	µA	T = 85 °C
Deep Sleep Mode, V_{DDD} = 3.6 to 5.5 V							
SID34	I_{DD29}	I^2C wakeup	–	15.0	–	µA	T = 25 °C, 5.5 V

Note
7. Usage above the absolute maximum conditions listed in Table 4 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 5. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2.0	5.0	mA	

Table 6. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F_{CPU}	CPU frequency	DC	–	48.0	MHz	$1.8 \le V_{DD} \le 5.5$
SID49	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	Guaranteed by characterization
SID50	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	25.0	µs	24 MHz IMO. Guaranteed by characterization
SID52	$T_{RESETWIDTH}$	External reset pulse width	1.0	–	–	µs	Guaranteed by characterization

I/O

Table 7. I/O DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	V_{IH}[8]	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID241	V_{IH}[8]	LVTTL input, $V_{DDD} < 2.7$ V	0.7× V_{DDD}	–	–	V	
SID242	V_{IL}	LVTTL input, $V_{DDD} < 2.7$ V	–	–	0.3 × V_{DDD}	V	
SID243	V_{IH}[8]	LVTTL input, $V_{DDD} \ge 2.7$ V	2.0	–	–	V	
SID244	V_{IL}	LVTTL input, $V_{DDD} \ge 2.7$ V	–	–	0.8	V	
SID59	V_{OH}	Output voltage high level	V_{DDD} –0.6	–	–	V	I_{OH} = 4 mA at 3 V V_{DDD}
SID60	V_{OH}	Output voltage high level	V_{DDD} –0.5	–	–	V	I_{OH} = 1 mA at 1.8 V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 4 mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 8 mA at 3 V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 3 mA at 3 V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2.0	nA	25 °C, V_{DDD} = 3.0 V

Note
8. V_{IH} must not exceed V_{DDD} + 0.2 V.

Table 7. I/O DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID65A	I_{IL_CTBM}	Input leakage current (absolute value) for analog pins	–	–	4.0	nA	
SID66	C_{IN}	Input capacitance	–	–	7.0	pF	
SID67	V_{HYSTTL}	Input hysteresis LVTTL	15.0	40.0	–	mV	$V_{DDD} \geq 2.7$ V. Guaranteed by characterization
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	200.0	–	–	mV	$V_{DDD} \geq 4.5$ V. Guaranteed by characterization
SID69	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100.0	µA	Guaranteed by characterization
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200.0	mA	Guaranteed by characterization

Table 8. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time	2.0	–	12.0	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time	2.0	–	12.0	ns	3.3 V V_{DDD}, Cload = 25 pF

XRES

Table 9. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C_{IN}	Input capacitance	–	3.0	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100.0	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100.0	µA	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for VSEL and CUR_LIM Pins

Table 10. PWM AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID140	$T_{PWMFREQ}$	Operating frequency	–	–	48.0	MHz	
SID141	$T_{PWMPWINT}$	Pulse width (internal)	42.0	–	–	ns	
SID142	T_{PWMEXT}	Pulse width (external)	42.0	–	–	ns	
SID143	$T_{PWMKILLINT}$	Kill pulse width (internal)	42.0	–	–	ns	
SID144	$T_{PWMKILLEXT}$	Kill pulse width (external)	42.0	–	–	ns	
SID145	$T_{PWMEINT}$	Enable pulse width (internal)	42.0	–	–	ns	
SID146	$T_{PWMENEXT}$	Enable pulse width (external)	42.0	–	–	ns	
SID147	$T_{PWMRESWINT}$	Reset pulse width (internal)	42.0	–	–	ns	
SID148	$T_{PWMRESWEXT}$	Reset pulse width (external)	42.0	–	–	ns	

I^2C

Table 11. Fixed I^2C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	10.5	µA	
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135.0	µA	
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310.0	µA	
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4	µA	

Table 12. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1.0	Mbps	

Memory

Table 13. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V_{PE}	Erase and program voltage	1.8	–	5.5	V	

Table 14. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$T_{ROWWRITE}$[9]	Row (block) write time (erase and program)	–	–	20.0	ms	Row (block) = 128 bytes
SID175	$T_{ROWERASE}$[9]	Row erase time	–	–	13.0	ms	
SID176	$T_{ROWPROGRAM}$[9]	Row program time after erase	–	–	7.0	ms	
SID178	$T_{BULKERASE}$[9]	Bulk erase time (32 KB)	–	–	35	ms	
SID180	$T_{DEVPROG}$[9]	Total device program time	–	–	7.0	seconds	Guaranteed by characterization
SID181	F_{END}	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F_{RET}[10]	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A		Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B		Flash retention. 85 °C < $T_A \leq$ 105 °C, 10K P/E cycles	3	–	–	years	Guaranteed by characterization

System Resources

Power-on-Reset (POR) with Brown Out

Table 15. Imprecise Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.45	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.40	V	Guaranteed by characterization
SID187	$V_{IPORHYST}$	Hysteresis	15.0	–	200.0	mV	Guaranteed by characterization

Table 16. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.64	–	–	V	Guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.40	–	–	V	Guaranteed by characterization

Note

9. It can take as much as 20 milliseconds to write to flash. During this time the device should not be Reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
10. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +105 °C ambient temperature range. Contact customercare@cypress.com.

SWD Interface

Table 17. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DDD} ≤ 5.5 V	–	–	14.0	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.8 V ≤ V_{DDD} ≤ 3.3 V	–	–	7.0	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T	ns	Guaranteed by characterization
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 18. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000.0	µA	

Table 19. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation	–	–	±2.0	%	With API-called calibration
SID226	$T_{STARTIMO}$	IMO startup time	–	–	12.0	µs	
SID229	$T_{JITRMSIMO3}$	RMS Jitter at 48 MHz	–	139.0	–	ps	

Internal Low-Speed Oscillator

Table 20. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO1}	ILO operating current at 32 kHz	–	0.30	1.05	µA	Guaranteed by characterization
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2.0	15.0	nA	Guaranteed by design

Table 21. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	2.0	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40.0	50.0	60.0	%	Guaranteed by characterization
SID237	$F_{ILOTRIM1}$	32-kHz trimmed frequency	15.0	32.0	50.0	kHz	±60% with trim.

Applications in Detail

Figure 8. Single Chip/Cable, Component Count =19

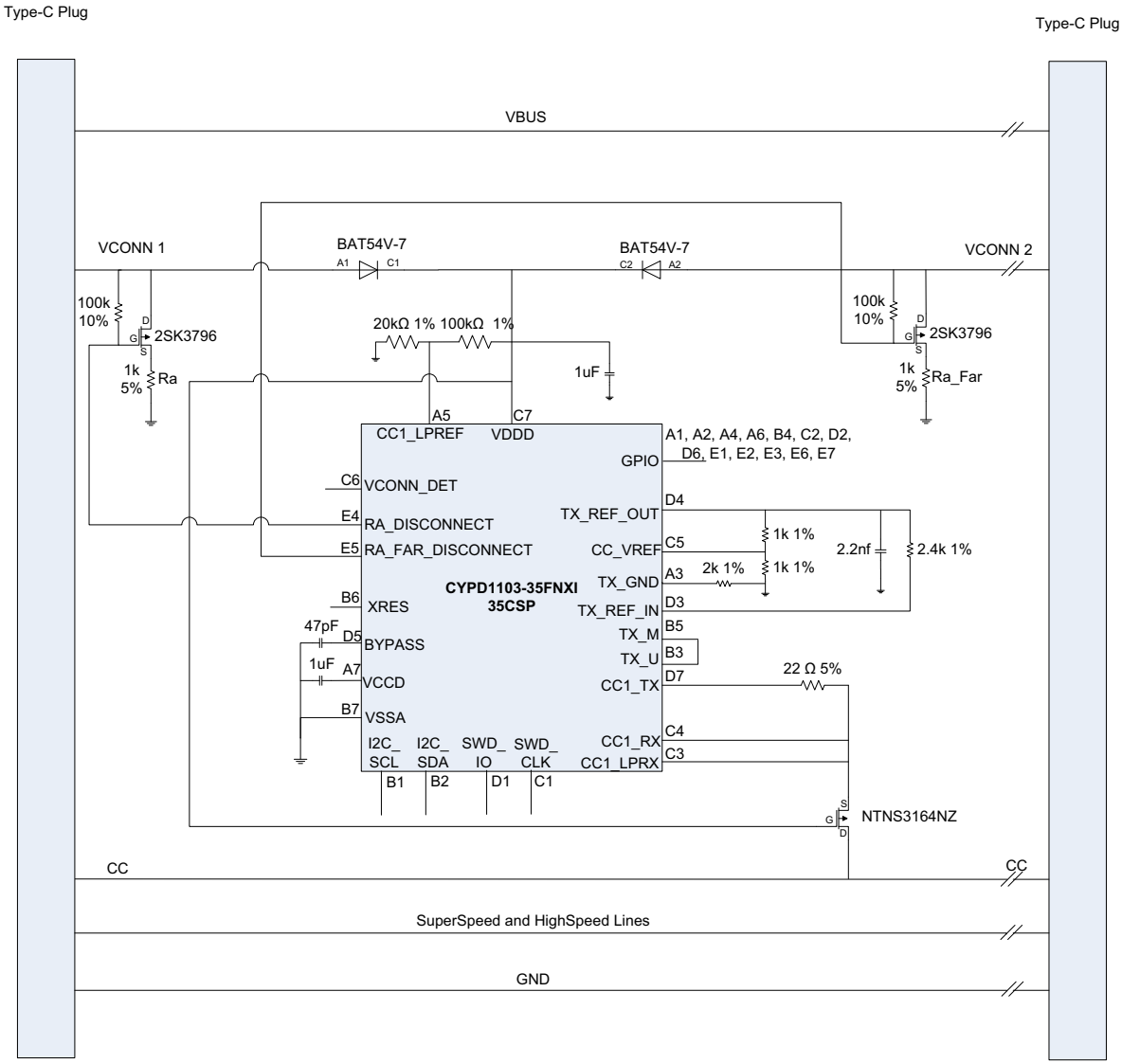


Figure 9. Single Chip/Cable, Component Count = 13

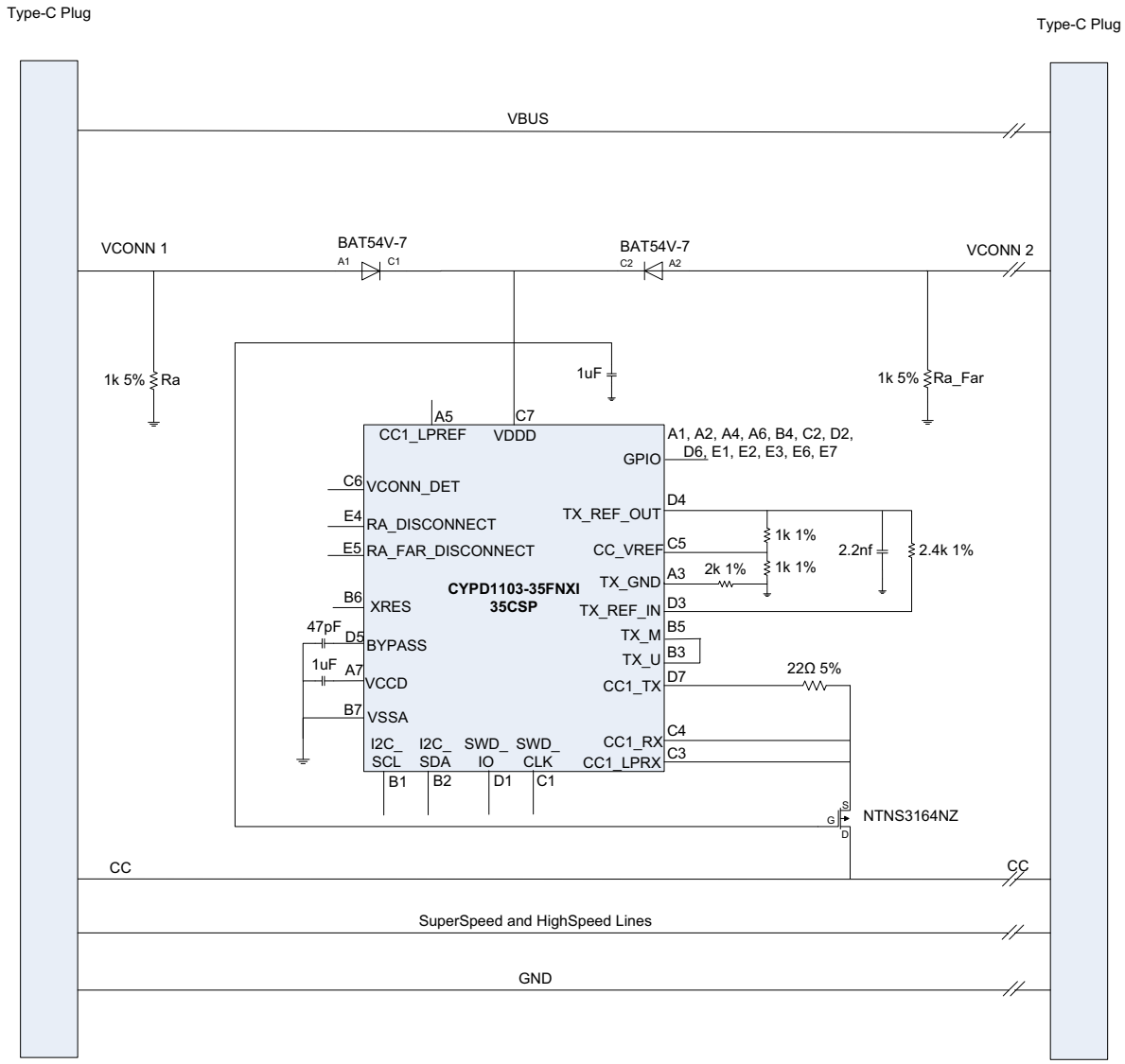


Figure 10. Two Chip/Cable, Component Count = 15/paddle

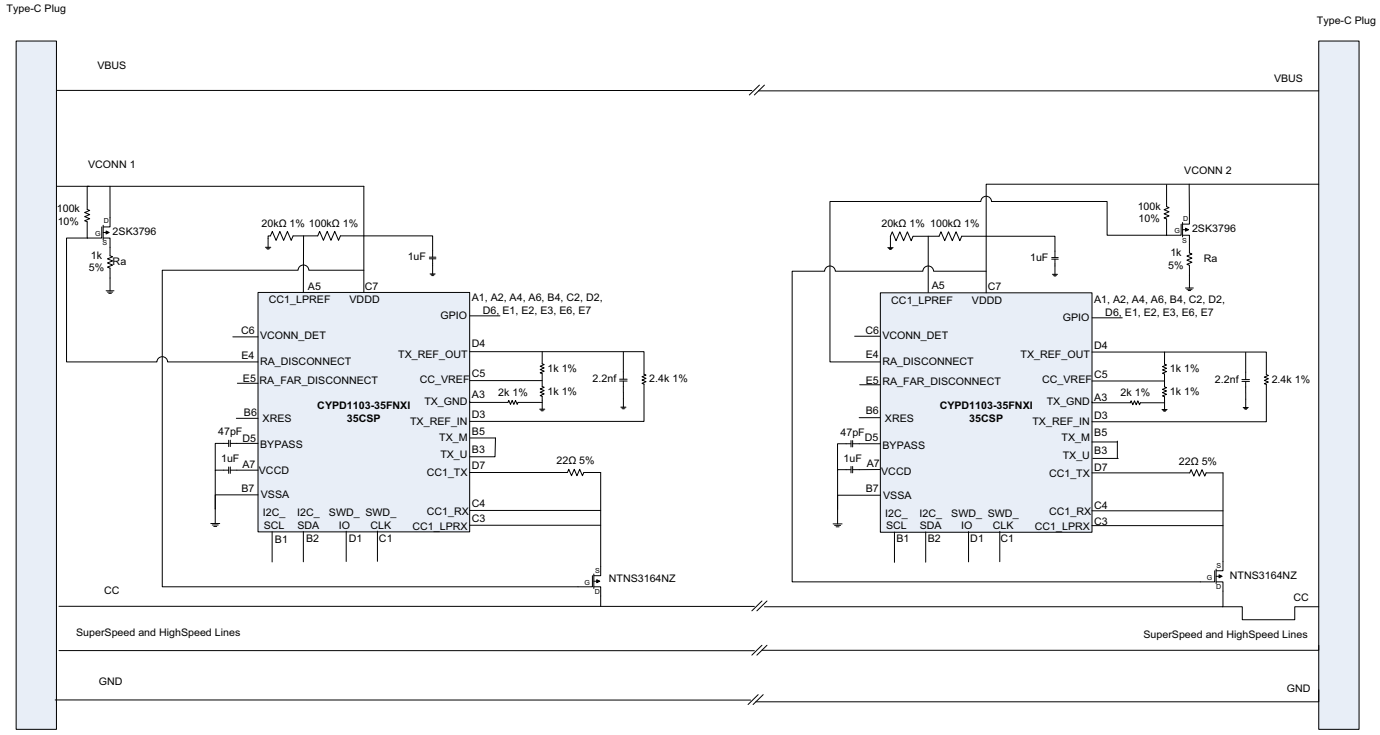


Figure 11. Two Chip/Cable, Component Count = 11/paddle

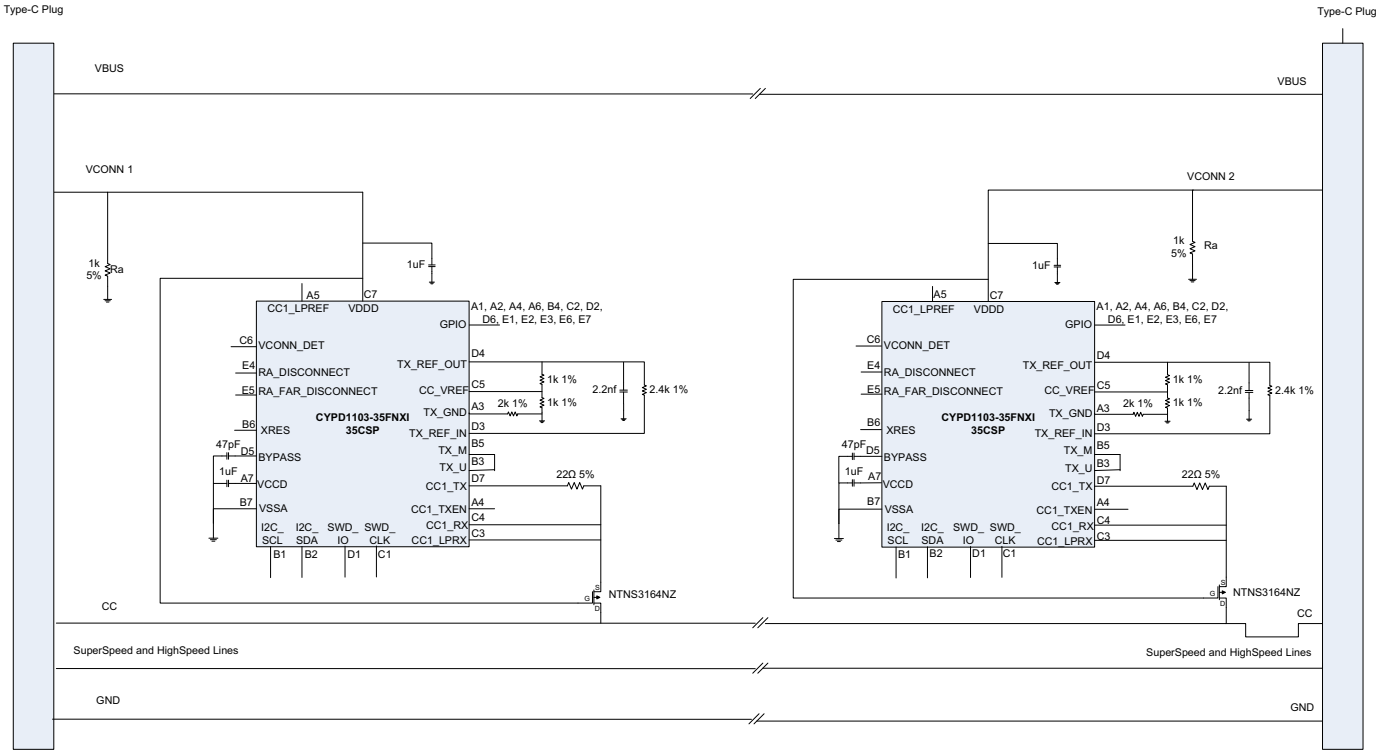


Figure 12. 16-pin SOIC Power Adapter Application Diagram

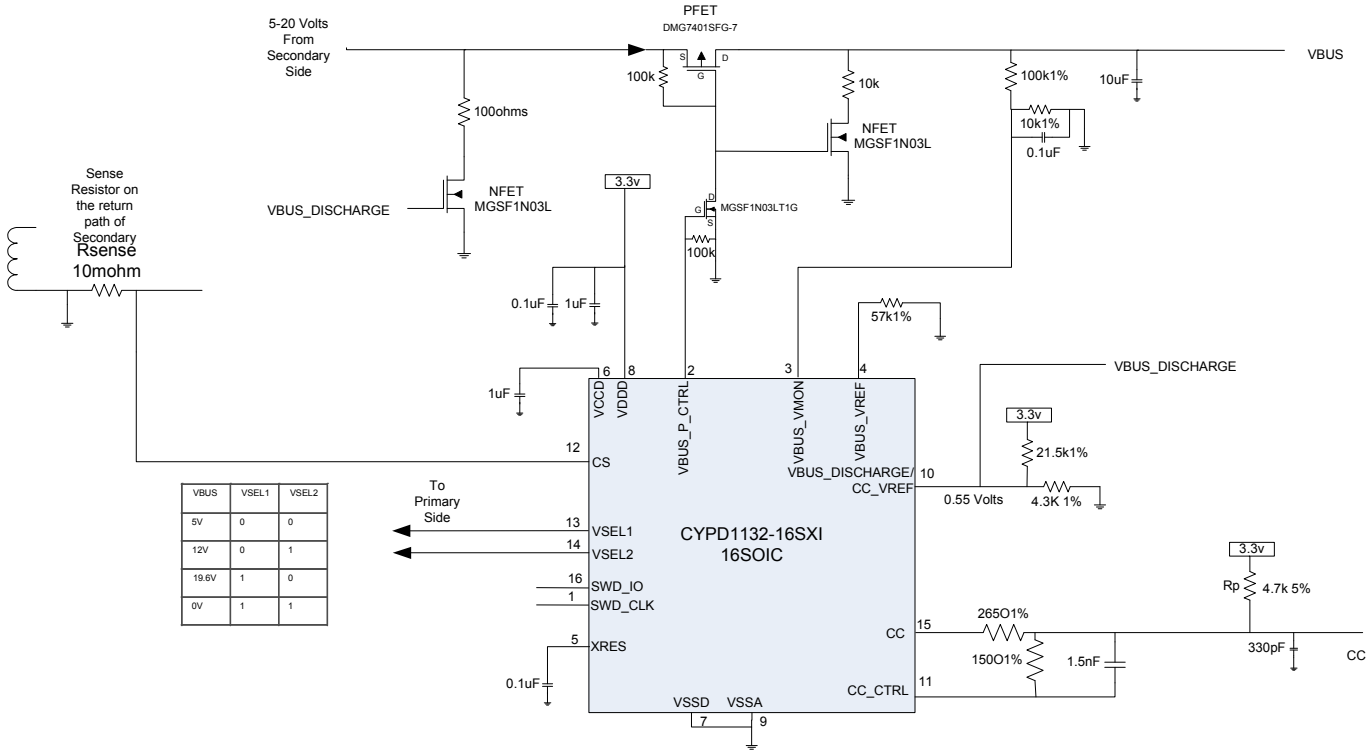


Figure 13. Notebook (DRP) Application Diagram

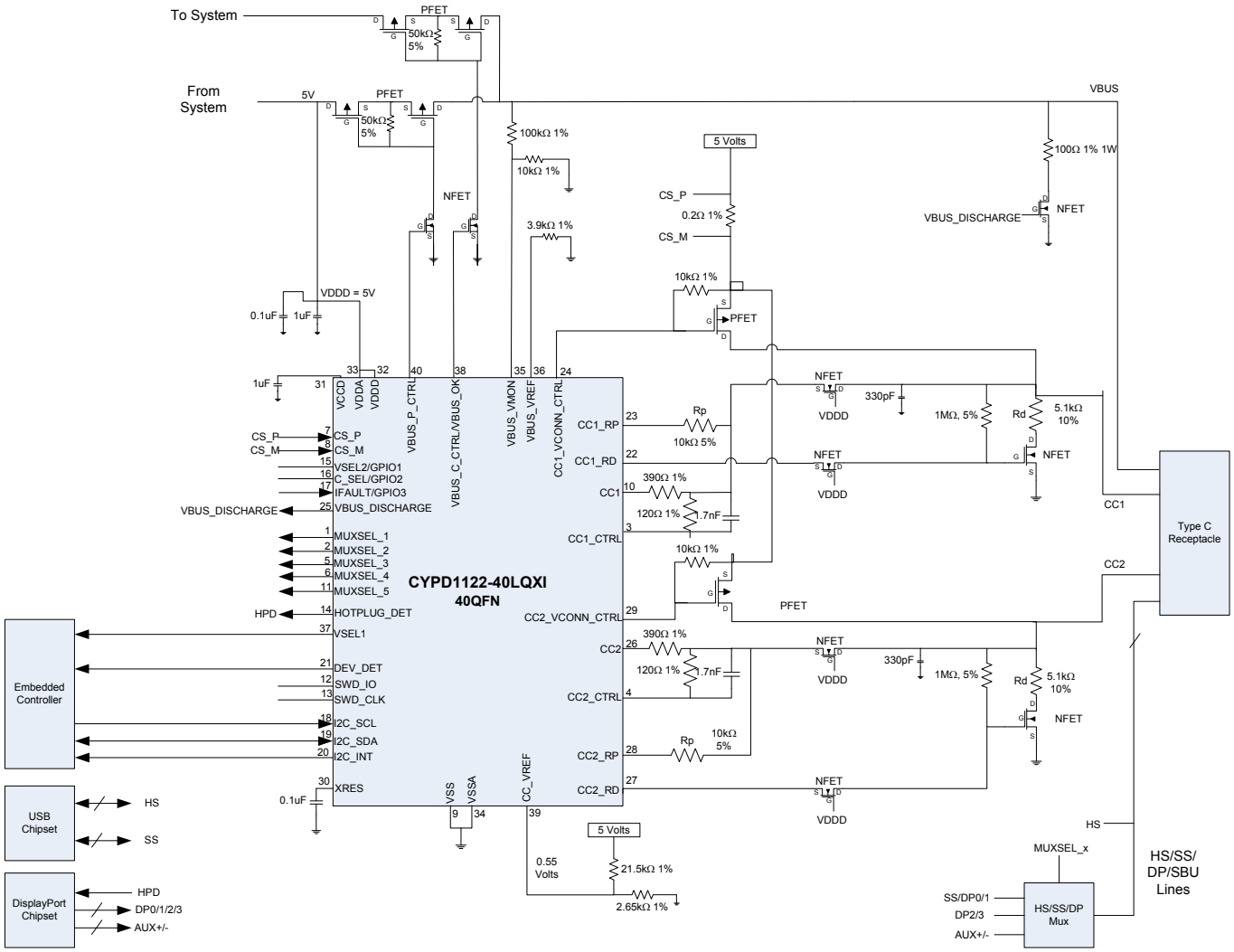


Figure 14. Notebook (DFP) Application Diagram

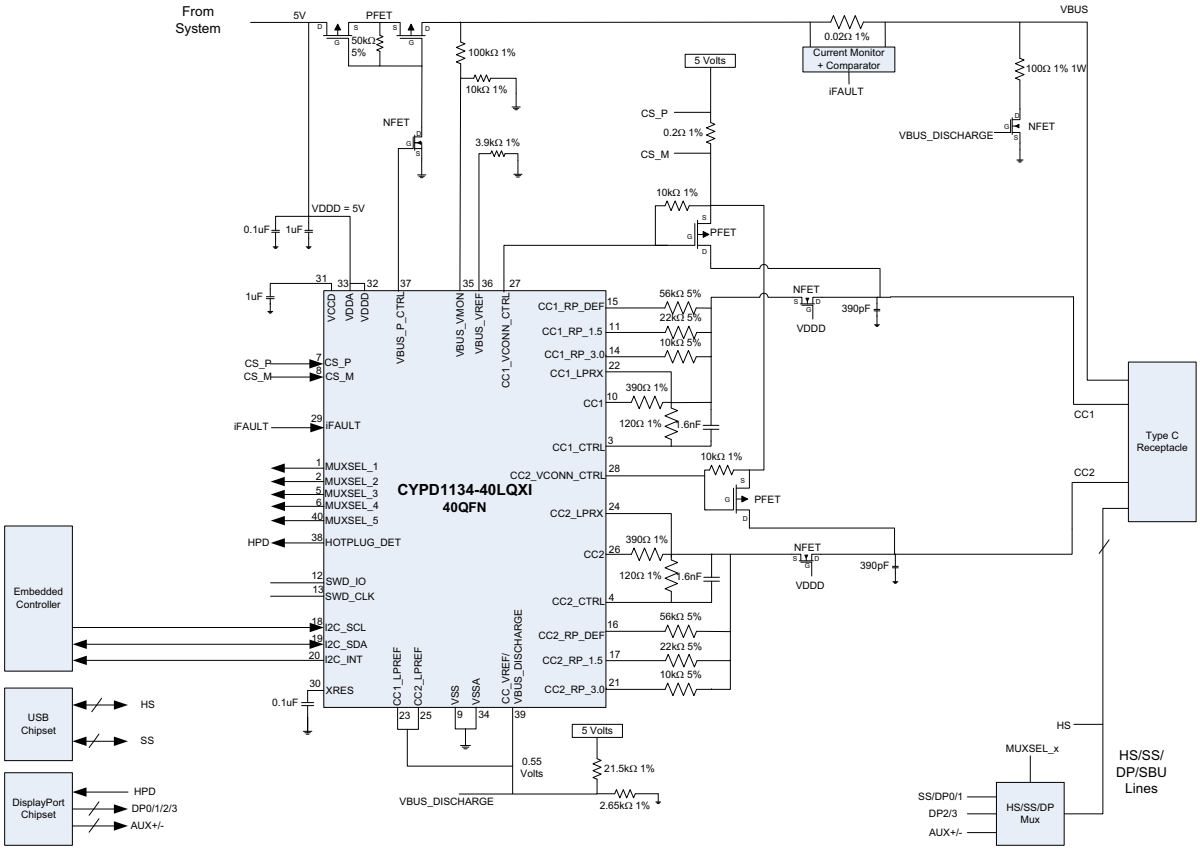
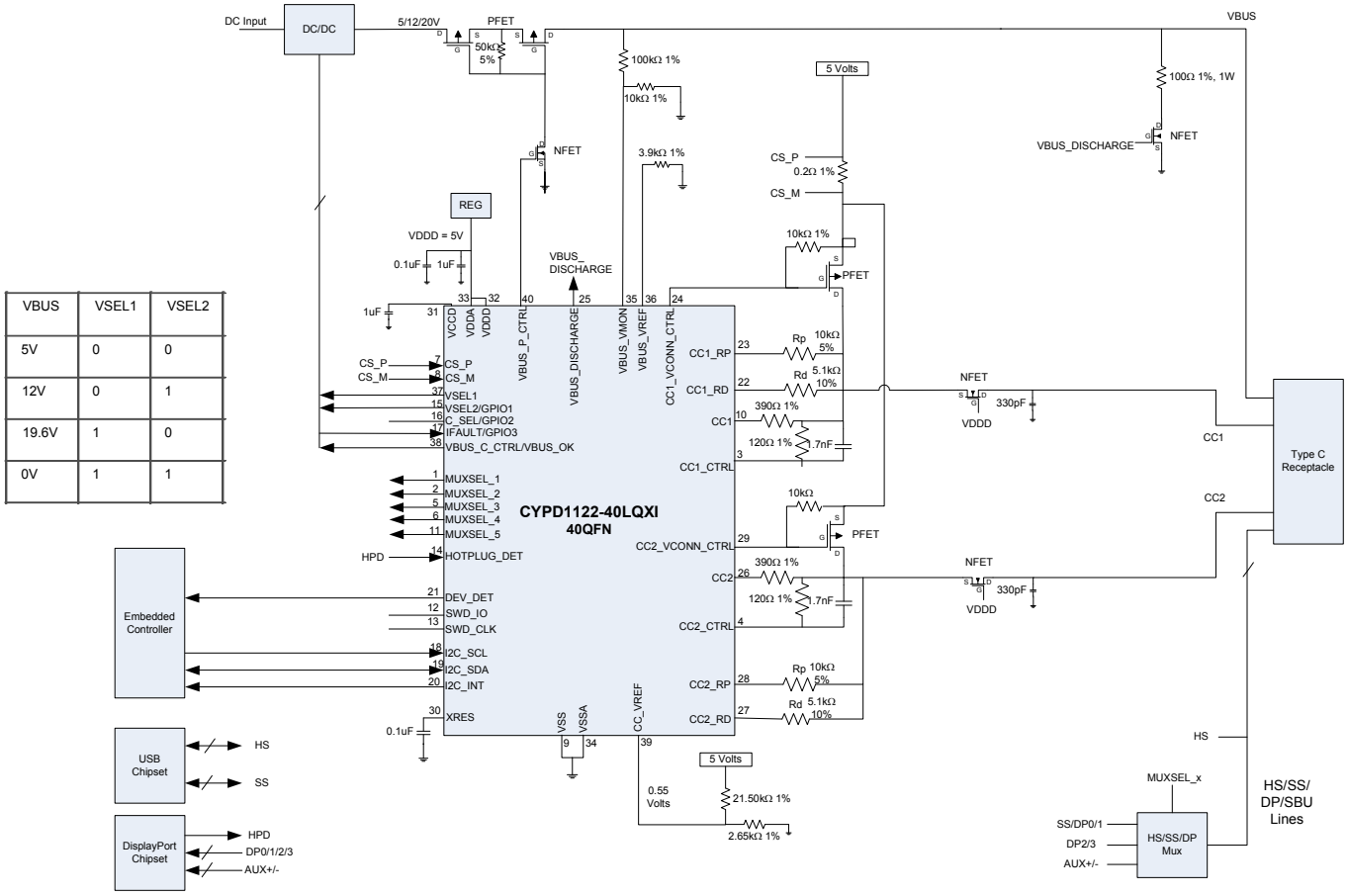


Figure 15. Monitor Application Block Diagram



VBUS	VSEL1	VSEL2
5V	0	0
12V	0	1
19.6V	1	0
0V	1	1

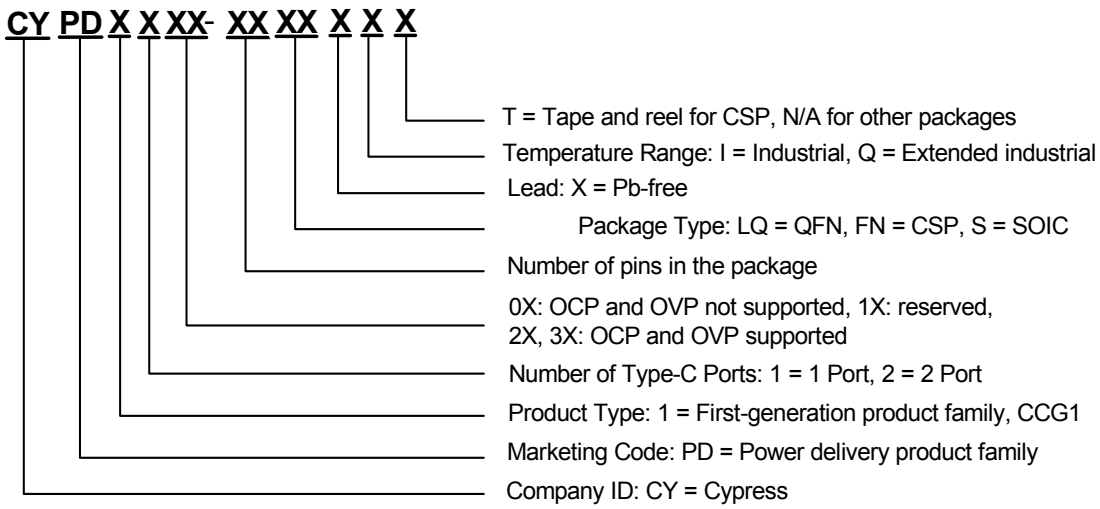
Ordering Information

The CCG1 part numbers and features are listed in the following table.

Table 22. CCG1 Ordering Information

Part Number[11]	Application	Type-C Ports[12]	Overcurrent Protection	Overvoltage Protection	Termination Resistor[13]	Role[14]	Package	Si ID
CYPD1103-35FNXIT	Cable, EMCA	1	No	No	R_a[15]	Cable	35-WLCSP[16]	0490
CYPD1131-35FNXIT	Notebook, Tablet, Smartphone	1	Yes	Yes	R_p[19], R_d[17]	DRP[20]	35-WLCSP[18]	0491
CYPD1121-40LQXI	Monitor	1	Yes	Yes	R_p[19], R_d[17]	DRP[20]	40-QFN[22]	0489
CYPD1122-40LQXI	Notebook	1	Yes	Yes	R_p[19], R_d[17]	DRP[20]	40-QFN[21]	048A
CYPD1134-40LQXI	Notebook, Desktop	1	Yes	Yes	R_p[19]	DFP[24]	40-QFN[23]	048B
CYPD1132-16SXI	Power Adapter	1	Yes	Yes	R_p[19]	DFP[24]	16-SOIC	0498
CYPD1132-16SXQ	Power Adapter	1	Yes	Yes	R_p[19]	DFP[24]	16-SOIC	0498

Ordering Code Definitions


CY PD X X XX- XX XX X X X
T = Tape and reel for CSP, N/A for other packages
Temperature Range: I = Industrial, Q = Extended industrial
Lead: X = Pb-free
Package Type: LQ = QFN, FN = CSP, S = SOIC
Number of pins in the package
0X: OCP and OVP not supported, 1X: reserved,
2X, 3X: OCP and OVP supported
Number of Type-C Ports: 1 = 1 Port, 2 = 2 Port
Product Type: 1 = First-generation product family, CCG1
Marketing Code: PD = Power delivery product family
Company ID: CY = Cypress

Notes
11. All part numbers support: Input voltage range from 1.8 to 5.5 V. Industrial parts support -40 °C to +85 °C, Extended Industrial parts support -40 °C to 105 °C.
12. Number of USB Type-C Ports Supported .
13. Default V_{CONN} Termination.
14. PD Role.
15. Type-C Cable Termination.
16. 35-WLCSP#1 pinout.
17. USB Device Termination.
18. 35-WLCSP#2 pinout.
19. USB Host Termination.
20. Dual Role Port.
21. 40-QFN#1 pinout.
22. 40-QFN#2 pinout.
23. 40-QFN#3 pinout.
24. Downstream Facing Port.

Packaging

Table 23. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A (40-QFN, 35-CSP)	Operating ambient temperature		–40	25.00	85	°C
T_J (40-QFN, 35-CSP)	Operating junction temperature		–40	–	100	°C
T_A (16-SOIC)	Operating ambient temperature		–40	25.00	105	°C
T_J (16-SOIC)	Operating junction temperature		–40	–	120	°C
T_{JA}	Package θ_{JA} (40-pin QFN)		–	15.34	–	°C/Watt
T_{JA}	Package θ_{JA} (35-CSP)		–	28.00	–	°C/Watt
T_{JA}	Package θ_{JA} (16-SOIC)		–	85.00	–	°C/Watt
T_{JC}	Package θ_{JC} (40-pin QFN)		–	02.50	–	°C/Watt
T_{JC}	Package θ_{JC} (35-CSP)		–	00.40	–	°C/Watt
T_{JC}	Package θ_{JC} (16-SOIC)		–	49.00	–	°C/Watt

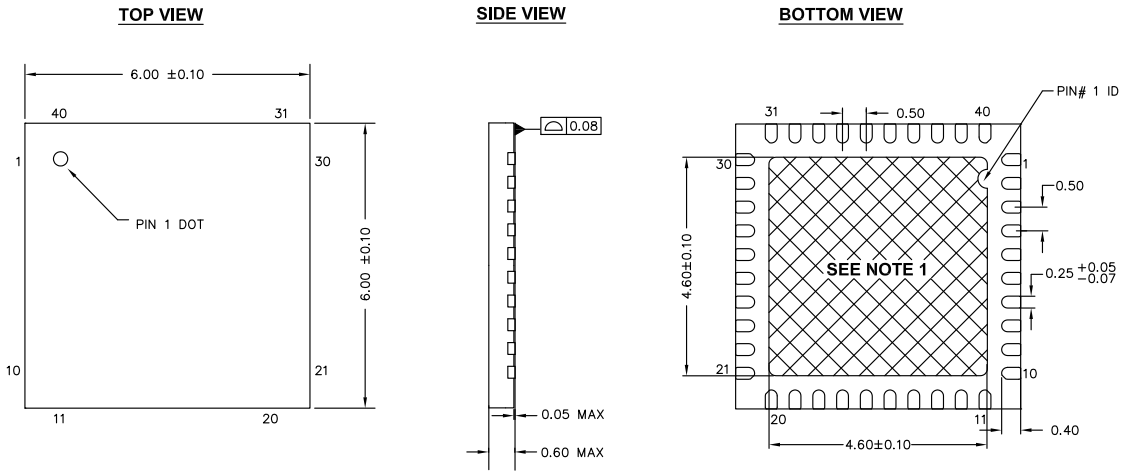
Table 24. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
16-pin SOIC	260 °C	30 seconds
40-pin QFN	260 °C	30 seconds
35-ball WLCSP	260 °C	30 seconds

Table 25. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
16-pin SOIC	MSL 3
40-pin QFN	MSL 3
35-ball WLCSP	MSL 1

Figure 16. 40-pin QFN Package Outline, 001-80659



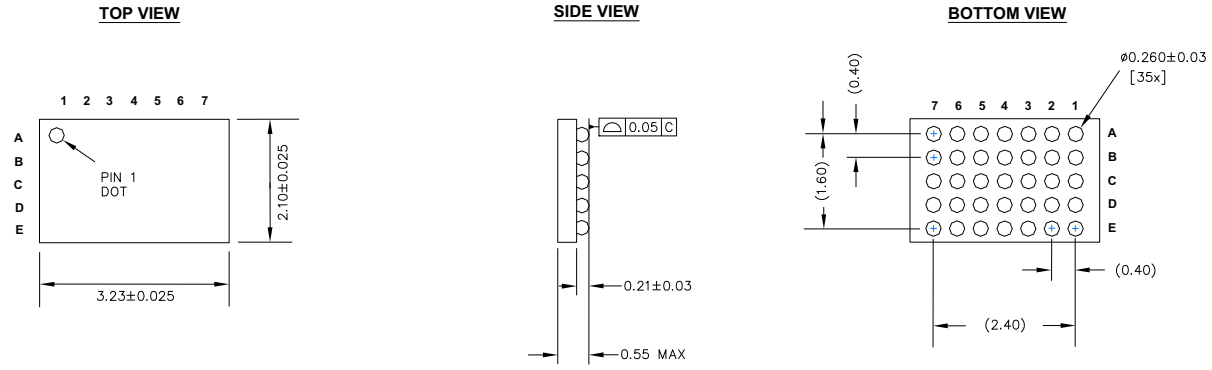
NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 **

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

Figure 17. 35-Ball WLCSP Package Outline, 001-93741

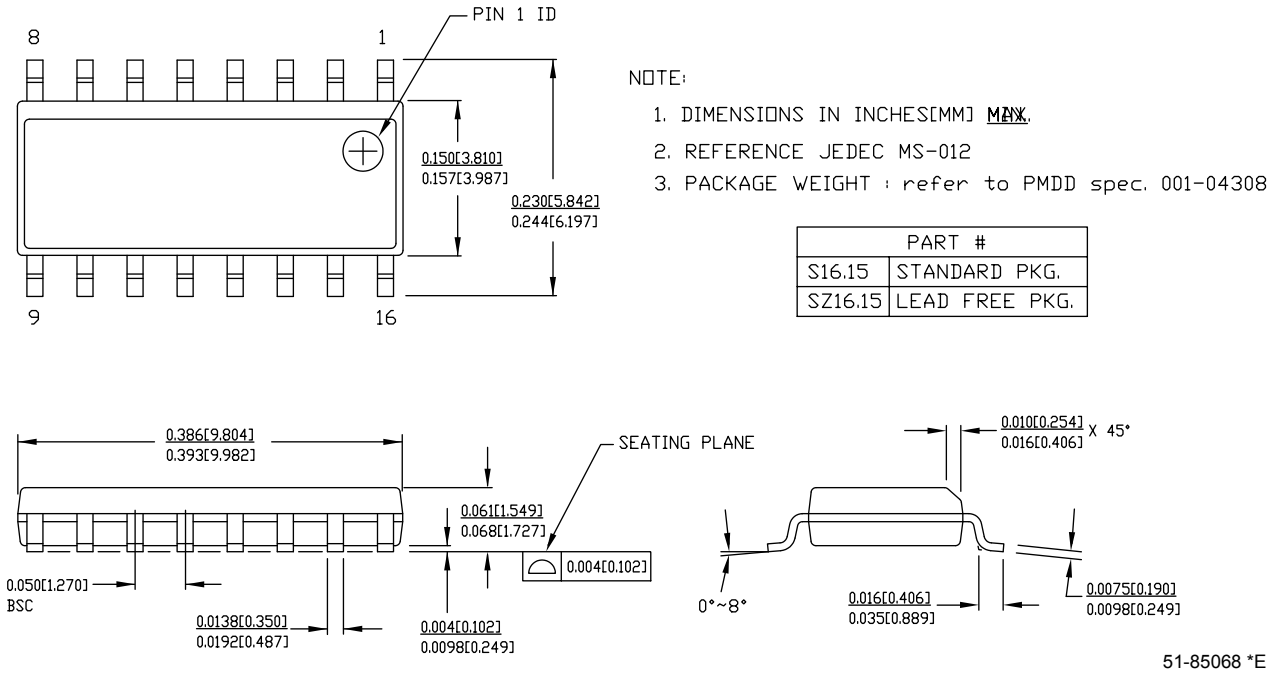


NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-93741 **

Figure 18. 16-pin SOIC (150 Mils) S16.15/SZ16.15 Package Outline, 51-85068



Acronyms

Table 26. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
CC	Configuration Channel
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	Current Sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO, DIO, SIO, USBIO
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller

Table 26. Acronyms Used in this Document *(continued)*

Acronym	Description
opamp	operational amplifier
OCP	Overcurrent protection
OVP	Overvoltage protection
PCB	printed circuit board
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UFP	upstream facing port
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
XRES	external reset I/O pin

Document Conventions

Units of Measure

Table 27. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision History

Description Title: CCG1 Datasheet USB Type-C Port Controller with Power Delivery Document Number: 001-93639				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4520316	MSMI	09/30/2014	New data sheet
*A	4531795	SJH	10/13/2014	Updated Functional Definition Updated Figure 8, Figure 9, Figure 10, Figure 11, Figure 14, Figure 13 Added Figure 15 Updated Pinouts Updated Power: Updated Figure 5, Figure 8 Updated Ordering Information Added Note 21 and referred the same note in 40-pin QFN corresponding to CYPD1122-40LQXI Added Note 23 and referred the same note in 40-pin QFN corresponding to CYPD1134-40LQXI
*B	4569912	SJH	11/21/2014	Updated Features Added 16-pin SOIC related information Updated Functional Definition Updated Pin Definitions Added Table 2 Updated Pinouts Updated Figure 2, Figure 4 Added Figure 3 Updated Power Updated Figure 5, Figure 8 Added Figure 6 Updated Electrical Specifications Updated Device Level Specifications Updated Memory Added Note 10 and referred the same note in F_{RET} parameter Added details corresponding to spec ID SID182B under F_{RET} parameter Updated Figure 14, Figure 13, Figure 15. Added Figure 12 and Figure 14 Updated Ordering Information Updated part numbers. Added a column “Si ID” Updated Packaging Updated Table 23 Updated details in maximum value column corresponding to T_A and T_J parameters Added 16-pin SOIC related information Updated Table 24
*C	4596141	SJH	12/14/2014	Updated Figure 6, Figure 14, Figure 16 Updated Table 7, Table 22
*D	4646123	SJH	02/04/2015	Updated pin definitions for 40-pin QFN and 35-ball WLCSP. Updated 40-pin QFN Pinout. Updated conditions for Device Level Specifications. Updated diagrams in Applications in Detail section. Updated Ordering Information.
*E	4686050	VGT	03/13/2015	Removed information about 28-pin SSOP Updated Table 2, Table 22, Table 23, Table 24, Table 25, Table 26 Updated Figure 2, Figure 5

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